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Mueller

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY.'S DOCKET: 00 P 9031 US

In re the application of:	)
Helmut Tews et al.	) Group Art: 2813
	)
Serial No.: 09/714,356	) Examiner: Chen, Jack SJ.
	)
Filing Date: November 16, 2000	)
	)
Title: NITROGEN IMPLANTATION USING A SHADOW EFFECT TO CONTROL GATE OXIDE THICKNESS IN DRAM SEMICONDUCTORS	)

INFORMATION DISCLOSURE DOCUMENT OF REFERENCES CITED IN COUNTERPART PCT US/01/46859 OF THE INTERNATIONAL SEARCH REPORT MAILED FEBRUARY 3, 2003

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

It is respectfully requested that the citations listed below and cited in the counterpart PCT application be considered by the Patent and Trademark Office and made of official record in the above-identified application.

US 4 454 524 A (SPENCE WENDELL)
12 June 1984 (1984-06-12)

US 6 080 682 A (IBOK EFFIONG E)
27 JUNE 2000 (2000-06-27)
the whole document

EP 0 884 776 A (SIEMENS AG)
16 December 1998 (1998-12-16)
The whole document.

In the opinion of the undersigned, the below-listed citations represents the closest art known to the undersigned during the preparation of the above-identified application. This citation may be material to the examination of the subject application and is therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R.§ 1.56 and 1.97.

A concise explanation of the relevance of the pertinent listed citations are set forth below.

U.S. Patent 4,454,524 is deemed pertinent for its disclosure of a semiconductor substrate of a predetermined conductivity type and having a channel region;

a gate structure overlying the channel region and defining channel region length and including a first, charge tunneling portion;

an insulating layer on the substrate and having an outer surface defining a well, the well having a base which defines the first, charge tunneling portion in the insulating layer and having walls extending from and sloping away from the base along the length of the channel region; and an impurity layer of the predetermined conductivity type underlying and approximately paralleling the walls of the well such that the layer forms a substrate surface adjacent concentration of impurities beneath the walls of the insulating layer for controlling parasitic inversion of the underlying substrate.

U.S. Patent 6,080,682 is deemed pertinent for its disclosure of A method of manufacturing a semiconductor device, comprising:

removing a thermal oxide layer from a main surface of a semiconductor substrate or of an epitaxial layer formed thereon;

depositing a blocking layer on the main surface of the semiconductor substrate or of the epitaxial layer formed thereon, after removing the thermal oxide layer;

providing a mask on the blocking layer, said mask containing a pattern having an

opening;

nitridating a section of the main surface beneath the opening;

removing the mask;

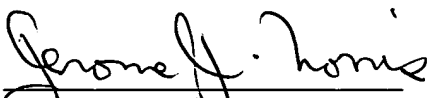
removing the blocking layer; and

forming a gate oxide over the nitridated section of the main surface.

EP 0 884 776 is deemed pertinent for its disclosure of a random access memory cell having a trench capacitor formed below the surface of the substrate. A shallow trench isolation is provided to isolate the memory cell from other memory cells of a memory array. The shallow trench isolation includes a top surface raised above the substrate to reduce oxidation stress.

Each item of the information contained in the Information Disclosure Statement was first cited in a counterpart foreign International Application No. PCT/US 01/46859 not more than three months prior to filing of the Information Disclosure Statement.

Respectfully submitted,



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March 4, 2003